

Panel 1

$$a = \{1, 2, 3, 4, 1, 2, 3, 0\}, b = \{0, 0, 0, 0, 0, 0, 0, 0\}$$

period is  $\underline{20} \mid 10$

$$\downarrow$$

$$\text{FFT}(1, 4, a, b)$$

$$\downarrow$$

$$a = \{2, 0, 1, 1, 5, \cancel{0}, 0\}, b = \{0, 1, 5, 7, 3, \cancel{0}, 1\}$$

$$2 + i + 0 \cos\left(\frac{10}{20}t\right) + 1 \sin\left(\frac{10}{20}t\right)$$

$$+ 1 \cos\left(\frac{20}{20}t\right) + 5 \sin\left(\frac{20}{20}t\right) +$$

$$+ 1 \cos\left(\frac{30}{20}t\right) + 7 \sin\left(\frac{30}{20}t\right)$$

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Panel 2

Last Time:

- Quizzes - by Friday
- telephone ✓
- multiplex ring ✓

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Panel 3

Switching

Slower switch

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Panel 4

Circuit Switching vs Packet Switching

Circuit switching: establish a "copper" path from  
A to B, then send data

Packet switching:  
break data into packets, send  
individually

pro/con circuit switch: long set up (10 sec), then  
fast speeds, no delays or congestion

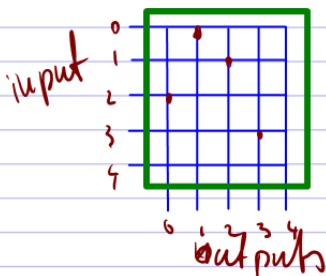
packet switching: more efficient use of resources  
but packets could get lost.

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Panel 5

Switches:

Crossbar switch      simplest switch



$n$ -inputs }  $n^2$   
 $n$ -outputs }  $n \times n$  cross points

Reduce cross points to

$$\frac{n \cdot (n-1)}{2}$$

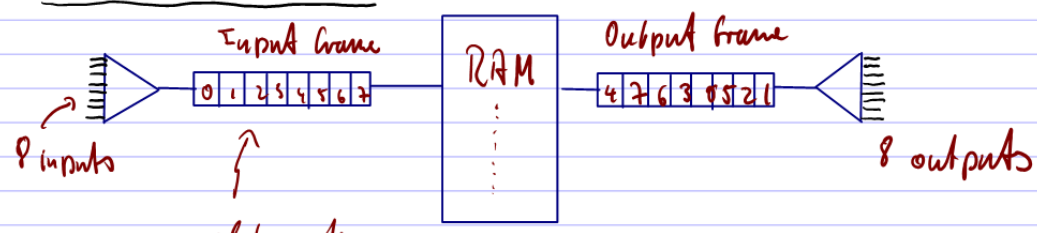
and use multistage switches

$\Rightarrow$  no longer used.

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Panel 6

Time Division Switch



$n$  slots with  $k$  bits

Time Slot Interchanger

Input frame goes into Interchanger in order  
 Read out different order

Need memory:  $n \times k + \text{extra for mapping table}$  ✓

Phone signals are sampled at 8000 samples per sec

$\Rightarrow$  1 sample per  $\frac{1}{8000} = 125 \mu\text{sec}$

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Panel 7

RAM chip must read in and out  $n$  samples every  $125 \mu\text{secs}$  ( $T_1$  line)

Suppose a memory read/write cycle takes  $T \mu\text{secs}$

$\Rightarrow 2nT = 125$

$\Rightarrow n = \frac{125}{2T}$

$T = 55 \mu\text{secs}$

$n = \frac{125 \cdot 10^{-6}}{2 \cdot 55 \cdot 10^{-9}} = \frac{125}{110} \cdot 10^3 = 1000$  lines

$T_2$  lines :  $4T_1 \approx \frac{1000}{4} = 250$  lines

$T_3$  :  $\frac{250}{7} \approx 40$  lines

$T_4$  :  $\frac{40}{6} \approx 6$  lines (400 Mbps)

Chip cycle time

20 Gbps  
 $\Rightarrow T$

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Panel 8

The Data Link Layer

...

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Panel 9

## The Data Link Layer

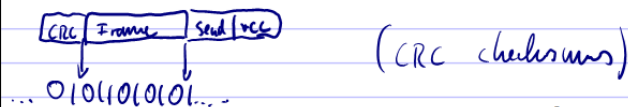
Transforms physical layer into a reliable link between nodes on one network.

Framing: divides bits into groups called frames

Physical address: e.g. MAC address of sender + receiver

Flow control: mechanism to know the transmiss. speed so not to overwhelm node

Error control: must detect + retransmit incorrect frames



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Panel 10

## Data Link Layer

① breaks bits into frames

- sends frame, could wait for acknowledge
- check frame for accuracy, request retransmit or send ackn.

How to break bits into frames?

... 0110000011110001100110 ...

① char count: add field for count<sup>8 4</sup>

if counter is invalid, can't recover any frame!

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Panel 11

011000...011110010011110010

② Insert flag code: 011110 flag byte

Problem: flag byte could occur in data

⇒ shifting: replace every 1111 with 11110

unshift: replace every 11110 with 1111

Next word segment...